CLAIMS

1. A system for controlling a FIFO, comprising:

a controller receiving a channel value indicating a number of channels used in a TDM data stream for transferring data, the controller varying data fill level threshold levels in the FIFO used for enabling read or write operations according to the number of channels value.

2. A system according to claim 1 including a TDM switch output enable signal for controlling the read or write operations.

3. A system according to claim 1 including a least significant bit signal disabling the read or write operations for a least significant bit for each time slot in the TDM data stream.

4. A system according to claim 1 including a clock position signal that enables the FIFO read or write operations for a single clock period of a TDM clock.

5. A system according to claim 1 including a clock synchronization circuit for synchronizing a FIFO serial read or write enable with a serial interface clock.

6. A system according to claim 1 including depth logic that varies a half_full FIFO threshold and a full FIFO threshold according to the number of channels used in the TDM data stream.

7. A system according to claim 1 wherein the depth logic identifies ranges for the number of channels used in the TDM data stream and doubles the half_full threshold and the full threshold for each higher range.

8. A system according to claim 1 wherein the controller comprises a state machine operating between different FIFO read or write states depending upon when data in the FIFO reaches the data threshold levels.

9. A system according to claim 8 wherein the state machine operates in a normal state where both a FIFO read enable and a FIFO write enable are activated when the FIFO has not reached a full or empty threshold.

10. A system according to claim 9 wherein the state machine operates in a FILL state where the FIFO read enable is deactivated and the FIFO write enable is activated when the FIFO has reached an empty threshold.

11. A system according to claim 10 wherein the state machine operates in a DEPLETE state where the FIFO read enable is activated and the FIFO write enable is deactivated when the FIFO has reached a full threshold.

12. A system according to claim 11 wherein the state machine generates an interrupt signal whenever the FIFO is in the FILL or DEPLETE state.

13. A system according to claim 1 including a TDM switch coupled to a first FIFO port and an external interface coupled a second FIFO port.

14. A system according to claim1 wherein the controller is used in a network processing circuit.

15. A system according to claim 1 including a loop back circuit that enables data from a TDM to serial FIFO to feed data back into a Serial to TDM FIFO.

16. A system according to claim 15 wherein the loop back circuit includes a first multiplexer for receiving serial input streams, a second multiplexer for receiving serial receive clocks, and a third multiplexer for receiving serial transmit clocks.

17. A system according to claim 1 including a count value indicating a data level for the FIFO, the controller using each increasingly significant bit in the count value to identify a half_full and full threshold for an increasing channel value range.

18. A system according to claim 1 wherein the TDM data stream is a T1 or E1 data stream and the channels are DS0 time slots.

19. A method for controlling how data is transferred in and out of a buffer, comprising:

identifying a time slot value for a number of time slots used for receiving or transmitting data in a frame;

determining one or more data fill level threshold values in the buffer according to the time slot value; and

controlling when data is written into and read out of the buffer according to a data level in the buffer in relation to the data fill level threshold values.

20. A method according to claim 19 assigning different data threshold values for different time slot value ranges.

21. A method according to claim 20 including doubling the data threshold values for each increasingly higher time slot value range.

22. A method according to claim 20 including:

receiving a count value representing the data fill level in the buffer; and

assigning the data fill level threshold values so that one bit in the count value is used for identifying a half full threshold for each one of the time slot value ranges and one bit in the count value is used for identifying a full threshold for each one of the time slot value ranges.

23. A method according to claim 19 including controlling writing or reading in the buffer according to an output enable from a TDM switch.

24. A method according to claim 19 including using a first buffer for writing in serial data and reading out channelized data and using a second buffer for writing in channelized data and reading out serial data.

25. A method according to claim 24 including assigning different data fill level threshold values for the first and second buffer according to the number of time slots used in each frame for the channelized data read out of the first buffer and written into the second buffer.

26. A method according to claim 24 including maintaining separate states for both the first and second buffer, the states including a FILL state when the data level reaches an empty threshold, a NORMAL state when the data level is between a full and empty threshold, and a DEPLETE state where the data level reaches a full threshold.

27. A method according to claim 26 including:

activating a buffer read enable signal and a buffer write enable signal in the NORMAL state;

deactivating the buffer read enable signal and activating the buffer write enable signal in the FILL state; and

activating the buffer read enable signal and deactivating the buffer write enable signal in the DEPLETE state.

28. A method according to claim 24 including reading out serial data from the second buffer and writing the serial data back into the first buffer.

29. A method according to claim 28 including generating a serial clock for both writing the serial data into the first buffer and reading the serial data out from the second buffer.

30. A method according to claim 29 including phase locking a frequency of the serial clock to a TDM clock.

31. A method according to claim 30 including controlling the serial clock according to a number of channels (N) and a N x 56K or N x 64K mode register value.

32. An electronic storage medium containing software for controlling how data is transferred in and out of a buffer, comprising:

code for identifying a time slot value for a number of time slots used for receiving or transmitting data in a frame;

code for determining one or more data fill level threshold values in the buffer according to the time slot value; and

code for controlling when data is written into and read out of the buffer according to a data level in the buffer in relation to the data fill level threshold values.

33. An electronic storage medium according to claim 32 including code for assigning different data threshold values for different time slot value ranges.

34. An electronic storage medium according to claim 33 including code for doubling the data threshold values for each increasingly higher time slot value range.

35. An electronic storage medium according to claim 33 including:

code for receiving a count value representing the data fill level in the buffer; and

code for assigning the data fill level threshold values so that one bit in the count value is used for identifying a half full threshold for each one of the time slot value ranges and one bit in the count value is used for identifying a full threshold for each one of the time slot value ranges.

36. An electronic storage medium according to claim 32 including code for controlling writing or reading in the buffer according to an output enable from a TDM switch.

37. An electronic storage medium according to claim 32 including code for using a first buffer for writing in serial data and reading out channelized data and using a second buffer for writing in channelized data and reading out serial data.

38. An electronic storage medium according to claim 37 including code for assigning different data fill level threshold values for the first and second buffer according to the number of time slots used in each frame for the channelized data read out of the first buffer and written into the second buffer.

39. An electronic storage medium according to claim 37 including code for maintaining separate states for both the first and second buffer, the states including a FILL state when the data level reaches an empty threshold, a NORMAL state when the data level is between a full and empty threshold, and a DEPLETE state where the data level reaches a full threshold.

40. An electronic storage medium according to claim 39 including:

code for activating a buffer read enable signal and a buffer write enable signal in the NORMAL state;

code for deactivating the buffer read enable signal and activating the buffer write enable signal in the FILL state; and

code for activating the buffer read enable signal and deactivating the buffer write enable signal in the DEPLETE state.

41. An electronic storage medium according to claim 37 including code for reading out serial data from the second buffer and writing the serial data back into the first buffer.

42. An electronic storage medium according to claim 41 including code for generating a serial clock for both writing the serial data into the first buffer and reading the serial data out from the second buffer.

43. An electronic storage medium according to claim 42 including code for phase locking a frequency of the serial clock to a TDM clock.

44. An electronic storage medium according to claim 43 including code for controlling the serial clock according to a number of channels (N) and a N x 56K or N x 64K mode register value.

45. A system for controlling how data is transferred in and out of a buffer, comprising:

means for identifying a time slot value for a number of time slots used for receiving or transmitting data in a frame;

means for determining one or more data fill level threshold values in the buffer according to the time slot value; and

means for controlling when data is written into and read out of the buffer according to a data level in the buffer in relation to the data fill level threshold values.

46. A system according to claim 45 including means for assigning different data threshold values for different time slot value ranges.

47. A system according to claim 46 including means for doubling the data threshold values for each increasingly higher time slot value range.

48. A system according to claim 46 including:

means for receiving a count value representing the data fill level in the buffer; and

means for assigning the data fill level threshold values so that one bit in the count value is used for identifying a half full threshold for each one of the time slot value ranges and one bit in the count value is used for identifying a full threshold for each one of the time slot value ranges.

49. A system according to claim 45 including means for controlling writing or reading in the buffer according to an output enable from a TDM switch.

50. A system according to claim 45 including means for using a first buffer for writing in serial data and reading out channelized data and using a second buffer for writing in channelized data and reading out serial data.

51. A system according to claim 50 including means for assigning different data fill level threshold values for the first and second buffer according to the number of time slots used in each frame for the channelized data read out of the first buffer and written into the second buffer.

52. A system according to claim 50 including means for maintaining separate states for both the first and second buffer, the states including a FILL state when the data level reaches an empty threshold, a NORMAL state when the data level is between a full and empty threshold, and a DEPLETE state where the data level reaches a full threshold.

53. A system according to claim 52 including:

means for activating a buffer read enable signal and a buffer write enable signal in the NORMAL state;

means for deactivating the buffer read enable signal and activating the buffer write enable signal in the FILL state; and

means for activating the buffer read enable signal and deactivating the buffer write enable signal in the DEPLETE state.

54. A system according to claim 50 including means for reading out serial data from the second buffer and writing the serial data back into the first buffer.

55. A system according to claim 54 including means for generating a serial clock for both writing the serial data into the first buffer and reading the serial data out from the second buffer.

56. A system according to claim 55 including means for phase locking a frequency of the serial clock to a TDM clock.

57. A system according to claim 56 including means for controlling the serial clock according to a number of channels (N) and an N x 56K or N x 64K mode register value.